

AMENDMENT TO THE CLAIMS

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strike through~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (currently amended) A Method-method for function testing an emulated logic circuit, comprising the steps of:

- ~~loading wherein~~ a model of a ~~the~~ logic circuit is ~~loaded into~~ a hardware emulator (EM) in a hardware description language, ~~wherein,~~
- putting the emulated logic circuit ~~is put~~ into an operating mode in which some or all of the flip-flops it contains, in particular with additional logic elements as interfacing circuitry, are functionally chained into one or more shift registers, and
- comparing ~~the~~ structural arrangement of the logic circuit in the hardware emulator (EM) ~~is compared with the~~ structural arrangement of the model of the logic circuit at least partially with the assistance of ~~this~~ the operating mode.

2. (currently amended) The Method-method according to ~~Claim-claim~~ 1, wherein further comprising the steps of:

- applying a test pattern ~~is applied to~~ inputs (~~ix~~) of the emulator (EM), the emulator inputs which simultaneously representing inputs of shift registers, and shifting the pattern ~~is shifted into~~ the shift registers by means of suitable pulsing,
- setting the emulated logic circuit ~~is set to~~ a standard operating mode whereby, one or more pulsing cycles ensue, and the circuit then re-sets ~~to the~~ an original operating mode,
- shifting the ensuing result pattern ~~is shifted by~~ means of suitable pulsing to emulator (EM) outputs (~~Ox~~) which simultaneously represent outputs of the shift registers, and carrying out a check ~~is carried out there~~ to determine whether the pattern matches an expected value, and
- using a check ~~this result is used to~~ compare the structural arrangement of the logic circuit in the hardware emulator (EM) ~~with the~~ structural arrangement of the model of the logic circuit.

3. (currently amended) ~~The method~~ The method according to ~~Claim-claim~~ Claim-claim 1, ~~wherein~~ further comprising the steps of:

- ~~applying a~~ applying a test pattern ~~is applied to~~ an emulator (EM) input, ~~the test pattern~~ representing an input of a shift register, and shifting the test pattern is shifted through the shift register by means of suitable pulsing,
- ~~checking an emulator (EM)-output, (Ox)-which simultaneously represents the output of this shift register, is checked for the appearance of this the test pattern or of the an inverted test pattern,~~
- ~~determining the a~~ determining a number of flip-flops in the shift register ~~is determined from the a number of pulsing sequences required for shifting through, and~~
- ~~using results of the step of determining in a comparison of this result is used to compare the structural arrangement of the logic circuit in the hardware emulator (EM) with the structural arrangement of the model of the logic circuit.~~

4. (currently amended) ~~The Method-method~~ The Method-method according to ~~Claim-claim~~ Claim-claim 3, ~~further comprising the steps of connecting wherein the an~~ further comprising the steps of connecting wherein the an output of a shift register (Ox) ~~is connected to the an input of a next adjacent shift register, and chaining (Ix+1) and all shift registers are chained into a single shift register by means of recursion.~~

5. (currently amended) ~~The Method-method~~ The Method-method according to ~~one of Claim-claim~~ one of Claim-claim 1, ~~further comprising the steps of: wherein~~ further comprising the steps of:

- in the event that the structural arrangement of the logic circuit in the hardware emulator (EM) ~~does not match the structural arrangement of the model, carrying out an analysis is carried out to determine the sources of such faults, and~~
- ~~automatically reloading the model of the logic circuit is automatically re-loaded into the hardware emulator (EM) with these sources of faults deactivated.~~

6. (currently amended) A ~~Device-device~~ Device-device for testing an emulated logic circuit, comprising:

- a hardware emulator (EM) for emulating a logic circuit present in the form of a model,
- a test pattern generator module (PG) for arranged to apply applying a test pattern to an input (Ix) of the hardware emulator (EM),

- a pulse generator arranged to inject for injecting a pulse into the hardware emulator ~~(EM)~~, and
- a test pattern checking module (PC) arranged to check for checking whether a bit pattern being applied to an output (~~Ox~~) of the hardware emulator ~~(EM)~~ matches an expected value, ~~the device additionally contains~~
- a module for comparing the a structural arrangement of the logic circuit in the hardware emulator (EM) with the a structural arrangement of the a model of the logic circuit at least partially with the assistance of an operating mode of the logic circuit in which some or all of the flip-flops it contains, in particular with additional logic elements as interfacing circuitry, are functionally chained into one or more shift registers.

7. (currently amended) The device according to claim 6, further comprising a module for determining the number of flip-flops in the shift register from ~~the a~~ a number of pulse sequences needed to shift a test pattern through the register and/or a module for briefly changing over the logic circuit to a standard operating mode for one pulse cycle or several pulse cycles while a test pattern is being shifted through the register.

8. (currently amended) The device according to claim 6, further comprising a module for chaining all the shift register into a single shift register by means of recursively connecting the output (~~Ox~~) of, ~~in each case,~~ one shift register to the input (~~Ix+1~~) of, ~~in each case,~~ a one next adjacent shift register.

9. (currently amended) The device according to claim 6 further comprising:

- a module for analyzing the sources of faults leading to a lack of matching between the structural arrangement of the logic circuit in the hardware emulator ~~(EM)~~ and the structural arrangement of the model, and
- a module for automatically loading the model of the logic circuit into the hardware emulator ~~(EM)~~ with these sources of faults deactivated.

10. (new) The device according to claim 6, further comprising a module for determining the number of flip-flops in the shift register from a number of pulse sequences needed to shift a test pattern through the register or a module for briefly

changing over the logic circuit to a standard operating mode for one pulse cycle or several pulse cycles while a test pattern is being shifted through the register.